## WHAT IS CLAIMED IS:

1	1. A method of tuning a voltage controlled oscillator comprising:				
2	measuring a frequency of oscillation of the voltage controlled oscillator;				
3	comparing the frequency of oscillation to a desired frequency;				
4	generating a logic signal; and				
5,	applying the logic signal to a resistor,				
6	wherein the resistor is coupled to a first capacitor and a second capacitor, the first				
7	capacitor is coupled to an inductor, and the second capacitor is coupled to a first supply terminal.				
1	2. The method of claim 2 wherein the second capacitor is a junction varactor.				
1	3. The method of claim 2 wherein the second capacitor is a MOS varactor.				
1	4. The method of claim 2 wherein the first supply terminal is ground.				
1	5. An integrated circuit having a voltage controlled oscillator comprising:				
2	a first inductor;				
3	a first capacitor coupled to the first inductor;				
4	a first varactor diode coupled to the first capacitor; and				
5	a first isolation resistor coupled to the first capacitor and the first varactor diode,				
6	wherein the first isolation resistor is configured to receive a control voltage.				
1	6. The integrated circuit of claim 5 further comprising:				
2	a second inductor;				
3	a second capacitor coupled to the first inductor;				
4	a second varactor diode coupled to the first capacitor;				
5	a second isolation resistor coupled to the second capacitor and the second varactor				
6	diode, wherein the second isolation resistor is configured to receive the control voltage;				
7	a first device having a drain coupled to the first inductor and a gate coupled to the				
8	second inductor; and				
9	a second device having a drain coupled to the second inductor and a gate coupled				
0	to the first inductor.				

1		7. The integrated circuit of claim 6 further comprising:				
2		a current source coupled to a source of the first device and a source of the second				
3	device.					
1		8. The integrated circuit of claim 7 wherein the current source is a common				
2	source device					
1		9. The integrated circuit of claim 7 wherein the first device and the second				
2	device and n-channel CMOS devices.					
1		10. An integrated circuit having a voltage controlled oscillator comprising:				
2	a first inductor;					
<u></u>		a second inductor;				
3 5 5 6 7		a first capacitor coupled to the first inductor;				
<u>.</u> 5		a second capacitor coupled to the first inductor;				
4		a third capacitor coupled to the first capacitor;				
<b>2</b> 7		a fourth capacitor coupled to the second capacitor;				
		a first isolation resistor coupled to the first capacitor and the third capacitor,				
8 9 9 0 1 1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1	wherein the fi	irst isolation resistor is configured to receive a control voltage;				
<u>1</u> 0		a second isolation resistor coupled to the second capacitor and the fourth				
<b>1</b> 1	capacitor, who	erein the second isolation resistor is configured to receive the control voltage;				
12	a first device having a drain coupled to the first inductor and a gate coupled to the					
13	second inductor; and					
14		a second device having a drain coupled to the second inductor and a gate coupled				
15	to the first inc	luctor.				
1		11. The integrated circuit of claim 10 further comprising:				
2		a current source coupled to a source of the first device and a source of the second				
3	device.					
1		12. The integrated circuit of claim 11 wherein the current source is a common				
2	source device					

1		13.	The integrated circuit of claim 11 wherein the first device and the second			
2	device and n-channel CMOS devices.					
1 2	are junction v	14.	The integrated circuit of claim 11 wherein the third and fourth capacitors s.			
1 2	are MOS vara	15.	The integrated circuit of claim 11 wherein the third and fourth capacitors			
1 2	signal.	16.	The integrated circuit of claim 11 wherein the control voltage is a logic			
<u>L</u> E1 E2	signal.	17.	The integrated circuit of claim 11 wherein the control voltage is an analog			
	transceiver.	18.	The integrated circuit of claim 10 wherein the integrated circuit is an RF			
1 12 13 13		19.	A phase-locked loop comprising:			
는 진2	2 a phase detector configured to receive a reference clock;					
<b>4</b> 3	a low-pass filter coupled to the phase detector;  a voltage-controlled oscillator coupled to the low-pass filter; and					
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5	a divider coupled between the voltage-controlled oscillator and the low-pass filter,					
6	wherein the voltage-controlled oscillator comprises:					
. 7			a first inductor;			
8			a second inductor;			
9			a first capacitor coupled to the first inductor;			
10			a second capacitor coupled to the first inductor;			
11			a third capacitor coupled to the first capacitor;			
12			a fourth capacitor coupled to the second capacitor;			
13			a first isolation resistor coupled to the first capacitor and the third			
14	capacitor, wh	erein tl	ne first isolation resistor is configured to receive a control voltage;			

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15	a second isolation resistor coupled to the second capacitor and the fourth
16	capacitor, wherein the second isolation resistor is configured to receive the control voltage;
17	a first device having a drain coupled to the first inductor and a gate
18	coupled to the second inductor; and
19	a second device having a drain coupled to the second inductor and a gate
20	coupled to the first inductor.

- 1 20. The integrated circuit of claim 19 wherein the first device and the second device and n-channel CMOS devices.
  - 21. The integrated circuit of claim 19 wherein the third and fourth capacitors are junction varactors.
  - 22. The integrated circuit of claim 19 wherein the third and fourth capacitors are MOS varactors.
    - 23. An electronic system comprising the phase-locked loop of claim 19.